

Tactyle 2.0 Release Announcement

February 7th 2011. Asygn is pleased to announce the immediate availability of Tactyle 2.0, a major revision of its successful, analog system level time-domain simulator. Plugging into standard analog design environments, Tactyle 2.0 addresses some of the most difficult verification issues in today's analog designs: circuits too large for SPICE; widely spaced time constants; high selectivity; complex, mixed-signal situations; massively repeated subcircuits (for imaging and memories, for example).

This release contains the following major enhancements:

- 4 x speed increase over Tactyle 1.x – benchmarks now show an average speed improvement of approximately 300x over standard VerilogA simulations.
- RF option, seamlessly allowing the efficient simulation of systems involving signals with widely differing frequency components, such as baseband modulation of an RF carrier.
- SC option, allowing Tactyle 2.0 to interface to a System C environment in order to, for example, co-simulate large digital systems in System C (such as processors, modulators, demodulators) with an Analog/Mixed-Signal sub-system in Tactyle 2.0.
- Improved support for buses, facilitating the capture of the digital portion of the Design Under Test.
- Full support for double and int data types, and also for the integration and derivative operations.
- Extensions to the Tactyle library, including a transformer, new analog-to-digital conversion components, and extra controlled sources.

Tactyle 2.0 is a key component in Asygn's verification offering, which includes the Fasyle frequency-domain simulator, associated libraries, example databases, and complementary consulting services.

If you have questions regarding this release or any other Asygn products and services, please contact:

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Asygn will be exhibiting at the DATE conference in Grenoble, France, from March 15-17 2011, stand 53 (1ST floor, next to the delegate coffee area).

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analog system design